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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/889,585	10/18/2001	Yasuaki Muto	P21298	2977

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EXAMINER	
NATNAEL, PAULOS M	
ART UNIT	**PAPER NUMBER**
2614	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/889,585	Applicant(s) MUTO ET AL.	
	Examiner Paulos M. Natnael	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 9* is/are rejected.

7)☒ Claim(s) *2-8 and 10-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: the claimed "said vertical frequency conversion processing circuit" includes "a vertical frequency conversion processing circuit", which appears to be exactly the same circuit. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hirano** et al., U.S. Pat. No. **6,144,412** in view of **Suzuki**, U.S. Pat. No. **5,315,327**.

Considering claim **1**, Hirano et al. discloses the following claimed subject matter, note;

a) a storage part storing the video signal, is met by Memory 2, fig.1;

c) an interlace-to-progressive conversion processing circuit converting, when the video signal output from said vertical frequency conversion processing circuit is an interlace

signal, the video signal from the interlace signal to a progressive signal, is met by IP converter 1, fig.1;

d) a scanning line conversion processing circuit *converting the number of scanning lines of the video signal output from said interlace-to-progressive conversion processing circuit, is met by Multiple scan convertor 3, fig.1;* (see col. 6, lines 37-44)

e) a horizontal pixel conversion processing circuit converting the number of horizontal pixels of the video signal output from said scanning line conversion processing circuit, is met *by Horizontal scaling unit 5,* fig.1; (see col. 6, lines 53-60)

f) a synchronous control circuit outputting a synchronous control signal for controlling operations of the vertical frequency conversion processing circuit, the interlace-to-progressive conversion processing circuit, the scanning line conversion processing circuit, and the horizontal pixel conversion processing circuit, is met by the Microprocessor 10 and Control Unit 11, fig.1; (see col. 7, lines 27-43)

Except for;

b) a vertical frequency conversion processing circuit outputting a write control signal for writing the input video signal in said storage part and a read control signal for reading the video signal stored in said storage part to said storage part for controlling

input/output of the video signal in/from said storage part while converting the vertical frequency of the video signal stored in said storage part;

Regarding b), Hirano et al discloses the memory 2 for holding data for interlace-to-progressive conversion. Hirano et al do not specifically disclose a frequency converter at the input of the system.

Suzuki discloses high scanning rate to standard scanning rate television signal converter wherein odd and even fields of a high-speed television signal are readout from field memories with time base of the fields being expanded. (see Figs. 2,6, and 8) Suzuki also discloses a memory controller that forms various control pulses for a write control and various control pulses for a readout control of the respective field memories on the basis of the reference synchronizing signal (REF Sync), the write clock, and the signal of the horizontal of scanning frequency. (col. 5, lines 3-13 and col. 8, line 62 thru col. 9, lines 2)

Therefore, it would have been obvious to those with ordinary skill in the art at the time the invention was made to modify the system of Hirano et al by providing the scanning rate converter of Suzuki in order for the system of Hirano to be able to convert a high-speed scanning rate signal into a standard scanning rate television signal or any other desired signal format and thus the system adapts to any type of input video signal of a different sort and converts it into the desired signal format, rendering the device of Hirano more versatile and useful to the user.

Considering claim **9:** Claim 9 is a method claim of claim 1 and, therefore, claim 9 is rejected for the same reasons as in claim **1.**

Allowable Subject Matter

4. Claims **2-8** and **10-16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art, Hatano et al, discloses a pixel conversion apparatus comprising a scanning line converter timing signal generator, sync signal generator and interpolation circuit. However, Hatano et al fails to disclose a video signal conversion device wherein said vertical frequency conversion processing circuit includes: a first line memory performing a write operation with reference to a first clock output from said synchronous control circuit while performing a read operation with reference to a second clock output from said synchronous control circuit to perform write and read operations of said video signal in response to a horizontal synchronizing signal of a first system output from said synchronous control circuit, and a vertical frequency conversion processing circuit operating with reference to said second clock for outputting said write control signal in response to said horizontal synchronizing signal of said first system and a vertical synchronizing signal of a first system output from said synchronous control circuit while outputting said read control signal in response to a horizontal synchronizing signal of a

second system and a vertical synchronizing signal of a second system output from said synchronous control circuit to convert the vertical frequency of the video signal output from said first line memory from the frequency of said vertical synchronizing signal of said first system to the frequency of said vertical synchronizing signal of said second system, said interlace-to-progressive conversion processing circuit includes: a second line memory operating with reference to said second clock for performing write and read operations of the video signal output from said vertical frequency conversion processing circuit in response to said horizontal synchronizing signal of said second system, and an interlace-to-progressive conversion circuit operating with reference to said second clock for converting the video signal output from said second line memory from an interlace signal to a progressive signal in response to said horizontal synchronizing signal of said second system, said scanning line conversion processing circuit includes: a third line memory operating with reference to said second clock for performing a write operation of the video signal output from said interlace-to-progressive conversion circuit in response to said horizontal synchronizing signal of said second system while performing a read operation of the written video signal in response to a horizontal synchronizing signal of a third system output from said synchronous control circuit, and a scanning line conversion circuit operating with reference to said second clock for converting the number of scanning lines of the video signal output from said third line memory in response to said horizontal synchronizing signal of said third system and said vertical synchronizing signal of said second system, and said horizontal pixel conversion processing circuit includes: a horizontal compression circuit operating with

reference to said second clock for compressing the number of horizontal pixels of the video signal output from said scanning line conversion circuit in response to said horizontal synchronizing signal of said third system, a fourth line memory performing a write operation with reference to said second clock while performing a read operation with reference to a third clock output from said synchronous control circuit to perform write and read ill operations of the video signal output from said horizontal compression circuit in response to said horizontal synchronizing signal of said third system, and a horizontal expansion circuit operating with reference to said third clock for expanding the number of horizontal pixels of the video signal output from said fourth line memory in response to said horizontal synchronizing signal of said third system, as in claims **2** and **10.**

wherein said interlace-to-progressive conversion includes a plurality of line memories so that the video signal is transferred from said field memory to at least one of said plurality of line memories in response to a delayed horizontal synchronizing signal lagging a horizontal synchronizing signal before interlace-to-progressive conversion in phase, for performing rotation of data between said plurality of line memories while performing synthesis of an interpolation line with data of said plurality of line memories and reading data of a current line from a line memory other than the line memory to which the video signal has been transferred among said plurality of line memories in response to said horizontal synchronizing signal, as in claims **3** and **10;**

the vertical frequency conversion includes generating a reading start address larger than a writing start address of said field memory when increasing the number of scanning lines by said scanning line conversion processing circuit for performing vertical expansion processing while generating a reading start address of a negative number when reducing the number of scanning lines by said scanning line conversion processing circuit for performing vertical reduction processing, as the reading start address of said field memory, and a black line insertion circuit inserting, when the reading start address of a negative number is generated by said address generation circuit, data of a black line by the value of the negative number, said synchronous control circuit includes a horizontal synchronizing signal generation circuit reducing the frequency of a horizontal synchronizing signal in reading of said field memory when performing said vertical expansion processing while increasing the frequency of the horizontal synchronizing signal in reading of said field memory when performing said vertical reduction processing, and said vertical frequency conversion processing circuit controls the read operation of said field memory in response to the horizontal synchronizing signal output from said horizontal synchronizing signal generation circuit, as in claims **4** and **12**;

wherein determining whether the video signal input in said vertical frequency conversion processing circuit is an odd field or an even field, said vertical frequency conversion processing circuit includes a field information storage circuit storing field information determined by said determination circuit in response to a vertical synchronizing signal before vertical frequency conversion and reading the stored field

information in linkage with the video signal stored in said field memory in response to the vertical synchronizing signal after vertical frequency conversion, said vertical frequency conversion processing circuit outputs the video signal to said interlace-to-progressive conversion circuit in response to the field information read by said field information storage circuit, and said interlace-to-progressive conversion processing circuit converts the video signal output from said vertical frequency conversion processing circuit from an interlace signal to a progressive signal by intra-field interpolation, as in claims **5** and **13**;

wherein creating a horizontal synchronizing signal forming the reference on the output side of said vertical frequency conversion processing circuit and on the input side of said scanning line conversion processing circuit, a vertical synchronizing signal generation circuit generating a vertical synchronizing signal with the horizontal synchronizing signal generated from said first horizontal synchronizing signal generation circuit, a second horizontal synchronizing signal generation circuit generating a horizontal synchronizing signal for creating a horizontal synchronizing signal forming the reference on the output side of said scanning line conversion processing circuit, and a selection circuit receiving a vertical synchronizing signal created from a vertical synchronizing signal of the video signal input in said vertical frequency conversion processing circuit and the vertical synchronizing signal output from said vertical synchronizing signal generation circuit for selecting and outputting the vertical synchronizing signal of said vertical synchronizing signal generation circuit when said vertical frequency conversion processing circuit performs vertical frequency conversion

while selecting and outputting the vertical synchronizing signal created from the vertical synchronizing signal of the video signal input in said vertical frequency conversion processing circuit when said vertical frequency conversion processing circuit performs no vertical frequency conversion as a vertical synchronizing signal for creating a vertical synchronizing signal forming the reference on the output side of said vertical frequency conversion processing circuit and forming the reference on the output side of said scanning line conversion processing circuit, and said first and second horizontal synchronizing signal generation circuits are reset with reference to the vertical synchronizing signal output from said selection circuit, as in claims **6** and **14**.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Balram et al., U.S. Patent No. **6,034,733** discloses a timing and control for deinterlacing and enhancement of non-deterministically arriving interlaced video data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ***Paulos M. Natnael*** whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paulos Natnael
May 3, 2004

PAULOS M. NATNAEL
PATENT EXAMINER